

ROHAN SRIDHAR PARTHASARATHY

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Master's student in Information and Network Engineering at KTH (Communication Track) with a background in Electronics. Specialized in Signal Processing, Telecommunications and Machine Learning. Oriented toward solving complex engineering challenges through the lens of AI-assisted engineering.

EDUCATION

- Master's of Science in Information and Network Engineering** Stockholm, Sweden
KTH Royal Institute of Technology 2025 - 2027
Relevant Coursework: Signal Theory, Digital Signal Processing, Digital Communication, Advanced Digital Communication, Queuing Theory and Teletraffic Systems, Wireless Networks
- Bachelor's of Technology in Electronics and Communication Engineering** Bengaluru, India
Amrita Vishwa Vidyapeetham 2021 - 2025
Relevant Coursework: Signals and Systems, Digital Signal Processing, Embedded Systems, Digital Communication, Machine Learning, Deep Learning

TECHNICAL SKILLS

- **Programming:** MATLAB, Python, C, C++. Verilog
- **Software and Tools:** Git, Azure DevOps, Kiro IDE, MS Office
- **Hardware and Embedded:** Siemens PADS, Cadence OrCAD, ModelSim, LTspice, LabVIEW, ESP32-S3

PROFESSIONAL EXPERIENCE

- Ericsson AB, Stockholm, Sweden - Quantum and Blockchain Summer Intern** Jun 2026 - Aug 2026
- Executed regression, sanity, and end-to-end testing for Ericsson Customer Acceptance (ECA), an enterprise blockchain platform for automated acceptance workflows for telecom operators.
 - Formulated test cases, identified edge case defects and tracked bug cycles using Azure DevOps, ensuring smooth sprint deployments.
 - Integrated Kiro IDE to enable AI-assisted testing workflows that accelerated test script generation, streamlined bug reproduction, and optimized overall QA execution speed.
- Aeronautical Development Establishment, Defence Research and Development Organisation, Bengaluru, India - Research Intern** Jun 2024 - Jul 2024
(India's national agency for military R&D, the Indian equivalent to FMV)
- Spearheaded the integration of multiple sensors and storage components using **UART, SPI and CAN** communication protocols, ensuring reliable data acquisition for the autopilot system of UAVs.
 - Implemented Verilog-based digital designs on FPGA, including **Kalman filters and PID control** algorithms.
 - Designed schematics in **Cadence OrCAD** and PCB layouts in **Siemens PADS** and generated Gerber files.

ACADEMIC PROJECTS

- End-to-End Physical Layer (PHY) Design for a QPSK Transceiver** Nov 2025 - Jan 2026
- Developed a QPSK transceiver in **MATLAB** comparing rectangular and Root Raised Cosine (RRC) pulse shaping for spectral efficiency.
 - Implemented synchronization algorithms with a **0.16%** training overhead, ensuring stable phase and timing recovery for **10,016-bit** packets.
 - Analyzed eye diagrams to measure the impact of noise and ISI, ensuring the receiver maintained a sufficient noise margin for reliable data detection.
- FIR Filter Design and Analysis for a Two-Channel Audio Equalizer** Nov 2025 - Dec 2025
- Completed the design and modeling of a complementary two-channel equalizer in **MATLAB**, developed a linear phase, Type 1 FIR filter that achieved a stop-band attenuation of **40 dB**.
 - Validated fixed-point viability for the ESP32-S3 platform by quantizing filter coefficients, and achieved an **SQNR of 56.5 dB**.
 - Implemented and validated the fixed-point structure and filter coefficients onto the **ESP32-S3** platform.
- Artifact Removal in EEG signals (Bachelor Thesis)** Feb 2024 - Sep 2025
- Managed the entire data acquisition process, collecting EEG signals from **twenty five participants** using the **Neuphony EEG Flex Cap (8-channel EEG device)** to build a real-world dataset for model development.
 - Developed an automated hybrid machine learning model (SVM) and Independent Component Analysis (ICA) in **Python** to remove ocular artifacts from EEG signals.
 - Successfully deployed and validated the model in a real-time EEG processing pipeline, confirming signal quality using quantitative metrics such as **Shannon Entropy, Fractal Dimension and PSD**.

EXTRA-CURRICULARS

Career Fair Host at THS Armada (Oct 2025 - Nov 2025) Managed corporate partner experience for industry leaders including **Mycronic** and **PTS (Post och Telestyrelsen)**. Coordinated logistics and on-site relations for Scandinavia's largest student career fair.